AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. - 8 **(Canceled)**

9. **(Previously Presented)** A signal modification integrated circuit suitable for use in connection with an optoelectronic device, the signal modification integrated circuit comprising:

a receive circuit configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the receive circuit has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the receive circuit being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates, wherein when each data rate in the plurality of automatically selectable data rates have been set but the loss of lock signal remains asserted the receive circuit is configured to cause the data stream to be passed through the signal modification integrated circuit without modification; and

a transmit circuit configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the transmit circuit has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the transmit circuit being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates.

10. **(Original)** The signal modification integrated circuit as recited in claim 9, wherein the signal modification integrated circuit comprises a clock data recover integrated circuit that includes an oscillator serving as a reference clock.

11. **(Original)** The signal modification integrated circuit as recited in claim 9, wherein the plurality of automatically selectable data rates includes the data rates: about 4 Gb/s; and, about 2 Gb/s.

12. **(Previously Presented)** The signal modification integrated circuit as recited in claim 9, wherein the receive circuit comprises one of: a receive CDR; a demultiplexer; and, a serializer.

13. **(Previously Presented)** The signal modification integrated circuit as recited in claim 9, wherein the transmit circuit comprises one of: a transmit CDR; a multiplexer; and, a deserializer.

14. – 16. **(Canceled)**

15. **(New)** An optoelectronic device comprising the signal modification integrated circuit as recited in claim 9, wherein the optoelectronic device is compatible with the Fibre Channel protocol.

16. **(New)** The optoelectronic device as recited in claim 15, wherein the optoelectronic device is compatible with at least one of: 2 gigabits per second Fibre Channel systems; and, 4 gigabits per second Fibre Channel systems.

17. **(New)** The optoelectronic device as recited in claim 15, wherein the optoelectronic device is compatible with an input data rate of about 10 gigabits per second.

18. **(New)** A transceiver module comprising the signal modification integrated circuit as recited in claim 9, further comprising a receive optical sub-assembly configured to receive an optical data signal and converts the optical data signal to an electrical data signal; and a transmitter optical sub-assembly configured to receive an electrical data signal and convert the electrical data signal to an optical data signal.

19. **(New)** The signal modification integrated circuit as recited in claim 9, wherein the integrated circuit includes a sub-circuit that provides clock and data recovery for a plurality of data rates.

20. **(New)** The signal modification integrated circuit as recited in claim 9, wherein the integrated circuit further comprises one of: multiplexer/demultiplexer circuitry; and serializer/deserializer circuitry.